What is claimed is:

1. A bit line contact structure, comprising:

a substrate having a transistor thereon, the transistor having a gate electrode, drain region, and source region;

a composite dielectric layer, sequentially having a first dielectric layer, barrier layer, and second dielectric layer, blanketly formed on the transistor, the first dielectric layer comprising a spin-coating material, the composite dielectric layer having an opening exposing the drain region; and

a conductive layer in the opening.

2. The structure as claimed in claim 1, wherein the first dielectric layer comprises polyimide, polysilsequioxane, or fluorinated polyimide.

3. The structure as claimed in claim 1, wherein the first dielectric layer is about 3000Å to 4000Å thick.

4. The structure as claimed in claim 1, wherein the barrier layer is SiN.

5. The structure as claimed in claim 1, wherein the barrier layer is about 100Å to 300Å thick.

6. The structure as claimed in claim 1, wherein the second dielectric layer comprises an oxide layer.

7. The structure as claimed in claim 1, wherein the second dielectric layer is about 1000Å to 3000Å thick.

8. The structure as claimed in claim 1, wherein the conductive layer is doped polycrystalline silicon, tungsten, aluminum, or copper.

9. The structure as claimed in claim 1, wherein the first conductive layer is about 2000Å to 4000Å thick.

10. A method of fabricating a bit line contact structure, comprising:

providing a substrate having a transistor thereon, the transistor having a gate electrode, drain region, and source region;

blanketly forming a first dielectric layer on the transistor using spin coating;

conformally forming a barrier layer covering the first dielectric layer;

blanketly forming a second dielectric layer on the barrier layer;

planarizing the barrier layer;

forming a patterned resist layer on the second dielectric layer;

etching the second dielectric layer using the patterned resist layer as an etching mask, forming an opening exposing the barrier layer;

removing the patterned resist layer;

removing the barrier layer in the opening;

etching the first dielectric layer using the second dielectric layer as an etching mask, forming a via; and

filling the via with a conductive layer.

11. The method as claimed in claim 10, further comprising removing the patterned resist layer using ashing.

12. The method as claimed in claim 10, wherein the first dielectric layer comprises polyimide, polysilsequioxane, or fluorinated polyimide.

13. The method as claimed in claim 10, wherein the first dielectric layer is about 3000Å to 4000Å thick.

14. The method as claimed in claim 10, wherein the conductive layer is doped polycrystalline silicon.

15. The method as claimed in claim 10, wherein the conductive layer is tungsten, aluminum, or copper.

16. The method as claimed in claim 10, wherein the conductive layer is about 2000Å to 4000Å thick.

17. The method as claimed in claim 10, wherein the barrier layer is SiN.

18. The method as claimed in claim 10, wherein the barrier layer is about 100Å to 300Å thick.

19. The method as claimed in claim 10, wherein the second dielectric layer comprises an oxide layer formed by a precursor having at least tetra ethoxysilane (TEOS).

20. The method as claimed in claim 10, wherein the second dielectric layer is initially about 3000Å to 6000Å thick.

21. The method as claimed in claim 10, wherein planarizing the second dielectric layer uses chemical mechanical polishing (CMP), leaving the second dielectric layer about 1000Å to 3000Å thick.

22. The method as claimed in claim 10, wherein etch selectivity of the first dielectric layer with respect to the gate electrode is reaching approximately 30 or greater.

23. The method as claimed in claim 10, wherein the gate electrode further comprises a spacer overlying a sidewall thereof.

24. The method as claimed in claim 10, wherein the spacer is SiN.